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On Chip CMOS Inverter Design Technique with Low Power and Fast Settling Time

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Abstract–*Performance of CMOS inverter depends on three important parameters of power, speed, and noise margin. In this paper effect of the W/L ratio of different transistors is analyzed by these three parameters. Effect of Change in technology is also analyzed in these three parameters. It has been observed that different technologies required different design techniques to get optimum results. The further role of capacitive load is also studied and it has been observed that at a specific capacitive load specific value of aspect ratio provides an optimum value of power dissipation with fast settling. Work done in this paper could be very helpful for circuit designer as this work has considered on-chip CMOS inverter under different load conditions and using different technologies.*

1. INTRODUCTION

CMOS inverter is one of the important members of the CMOS family. It is useful applications in many electronic circuits such as noise suppressors and oscillators.

A decade before power dissipation was not an important design parameter in electronic circuit design. Since the last one decayed, due to development in VLSI design technique electronic circuit are more compact and battery operated. Hence power is an important parameter.

In this paper, the basic topology of CMOS inverter is analysis for power optimization with a reasonable value of other parameters like settling time, power optimization, and noise margin.

In process of reducing power supply current requirements to be reduced but that will affect severely to settling time and load driving capability of an inverter. In this paper rigorous exercise is done to find out optimum value of the expected ratio of transistors that provides low power with reasonable values of other parameters.

Designing is been done using different technologies and different values of capacitive loads. So the effect of change of technology and capacitive load can also be analyzed on parameters like power optimization, settling time and noise margin.

In this field author A.S. Chakraborty Atel has given the noise margin parameters of a CMOS inverter circuit in the sub-threshold regime have been analyzed thoroughly with respect to a variable supply voltage, transistor strength, and temperature; without neglecting the significant DIBL and body bias effects. But knowledge of power optimization and settling time was incomplete. So in this theory, our research paper consist design of CMOS inverter with different technologies and different values of capacitive loads. So the effect of change of technology and the capacitive load is analyzed on parameters like settling time, power optimization and noise margin.

Power dissipation in c-mos inverter

Power dissipation considerations have become important not only from the reliability point of view but they have assumed greater importance by the advent of portable battery-driven devices like laptops, cell phones, PDAs etc.

2. COMPONENTS OF POWER DISSIPATION

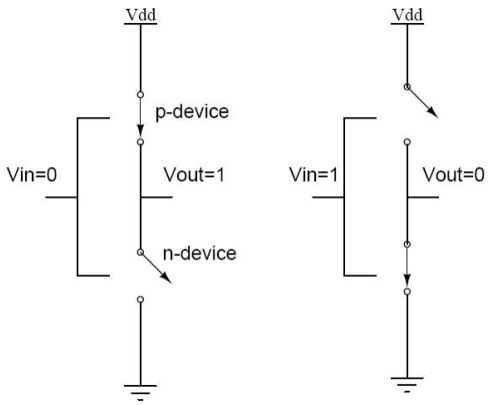
Unlike bipolar technologies, here a majority of power dissipation is static, the bulk of power dissipation in properly designed CMOS circuits is the dynamic charging and discharging of capacitances. Thus, a majority of the low power design methodology is dedicated to reducing this predominant factor of power dissipation.

There are three main sources of power dissipation:

- Static power dissipation (PS)
- Dynamic power dissipation (DS)
- Short circuit power dissipation (PSC)

3. STATIC POWER DISSIPATION

Consider the complementary CMOS gate. Shown

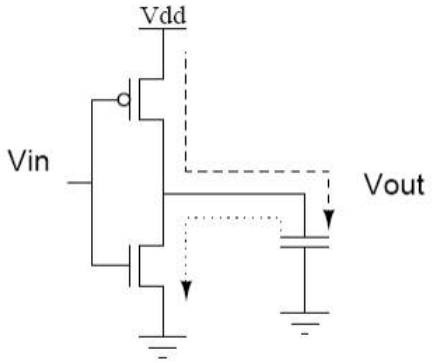


When input = '0', the associated n-device is off and the p-device is on. The output voltage is VDD or logic '1'. When the input = '1', the associated n-device is on and the p-device turns off. The output voltage is '0' volts or VSS. It can be seen that one of the transistors is always off when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no DC current path from VDD to vs., the resultant quiescent (steady-state) current, and hence power PS, is zero.

$$P_S = i_{leakage} * V_{DD}$$

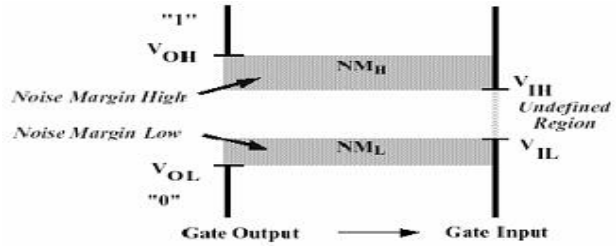
4. DYNAMIC POWER DISSIPATION

During switching, either from '0' to '1' or, alternatively, from '1' to '0', both n- and transistors are on for a short period of time. This results in a short current pulse from VDD to VSS. Current is also required to charge and discharge the output capacitive load. The current pulse from VDD to VSS results in a 'short-circuit' dissipation that is dependent on the input rise/fall time, the load capacitance and the gate design.



5. NOISE MARGINAL AND SETTLING TIME OF C-MOSS INVERTER

Noise margin allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected. The specification most commonly used to specify noise margin (or noise immunity) is in terms of two parameters- The LOW noise margin, NML, and the HIGH noised margin, NMH. NML is defined as the difference in magnitude between the maximum low output voltage of the driving gate and the maximum input LOW voltage recognized by the driven gate



$$NM_L = | V_{ILmax} - V_{OLmax} |$$

The value of NMH is difference in magnitude between the minimum HIHG output voltage of the driving gate and the minimum input HIGH voltage recognized by the receiving gate. Thus,

$$NM_H = | V_{OHmin} - V_{IHmin} |$$

Where,

VIH min = minimum HIGH input voltage

VIL max = maximum LOW input voltage

VOH min= minimum HIGH output voltage

VOL max= maximum LOW output voltage.

6. SETTLING TIME OF CMOS INVERTER

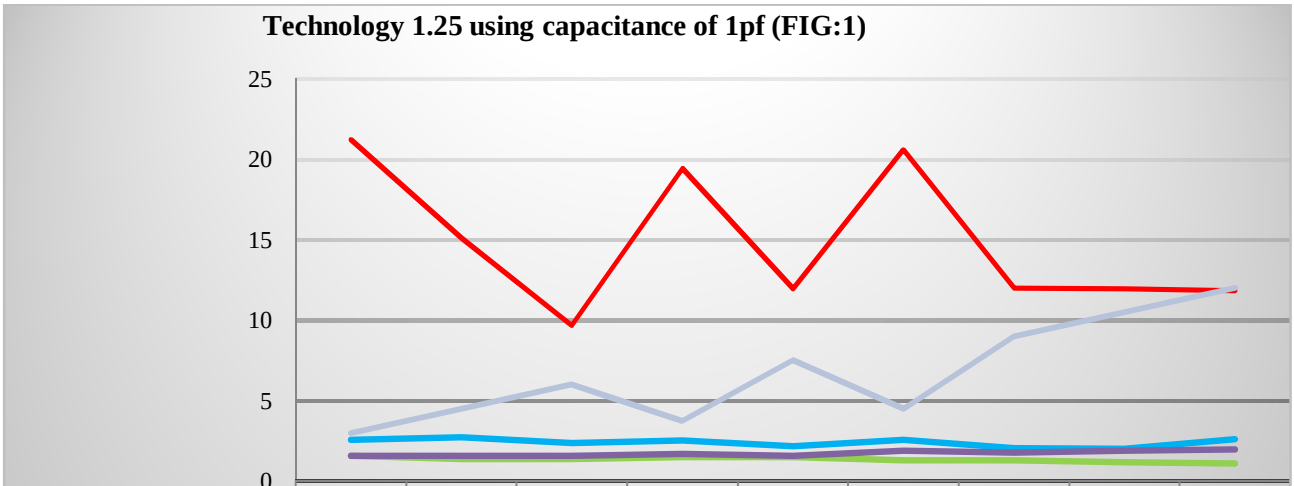
Rise time is defined as the time for a waveform to rise from 10% to 90% of its steady-state value. Fall time is defined as the time for a waveform to fall from 90% to 10% of its steady state value.

Indeed, by changing the relative widths of the NMOS to the PMOS, you can change the relationship between the rise and fall times. Assuming the size of the NMOS is given: if the rise time is faster than the fall time, you have wasted space by making the PMOS unnecessarily large without making the circuit as a whole run faster (it's limited by fall time). If the fall time is faster, you may be limiting the maximum frequency of the circuit, but depending on your particular needs, that might be acceptable, and the area gain may make it worth the time asymmetry.

7. EFFECT OF ASPECT RATIO OF TRANSISTORS ON POWER NOISE MARGIN AND SETTLING TIME WITH LOAD

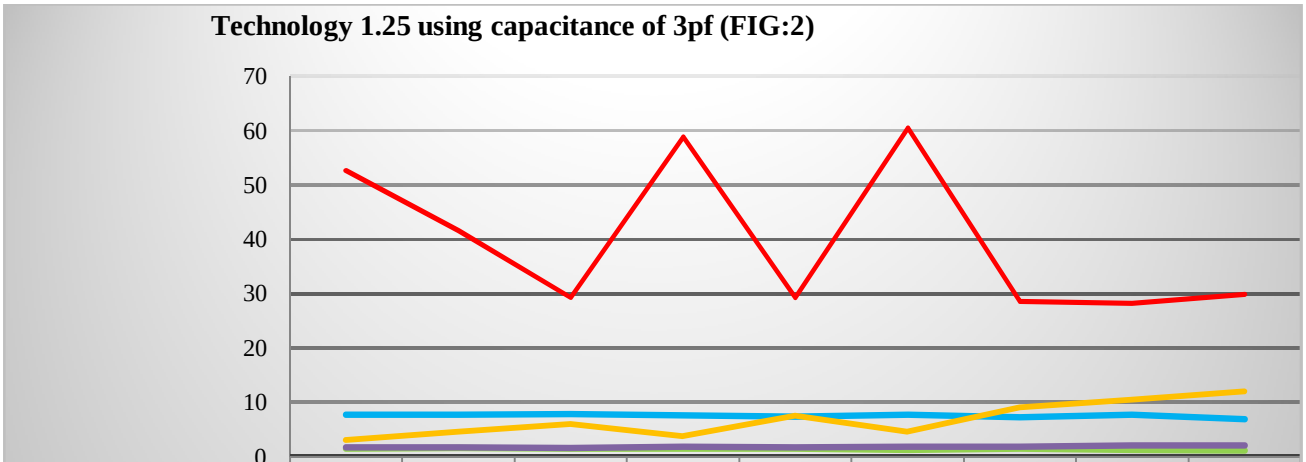
Under our research work, we have considered different aspects ratios of the PMOS and NMOS transistors of CMOS inverter.

Under different values of aspect ratios, we have seen variations in power, noise margin, area and settling time. This exercise has been done with different technologies and under different load conditions.



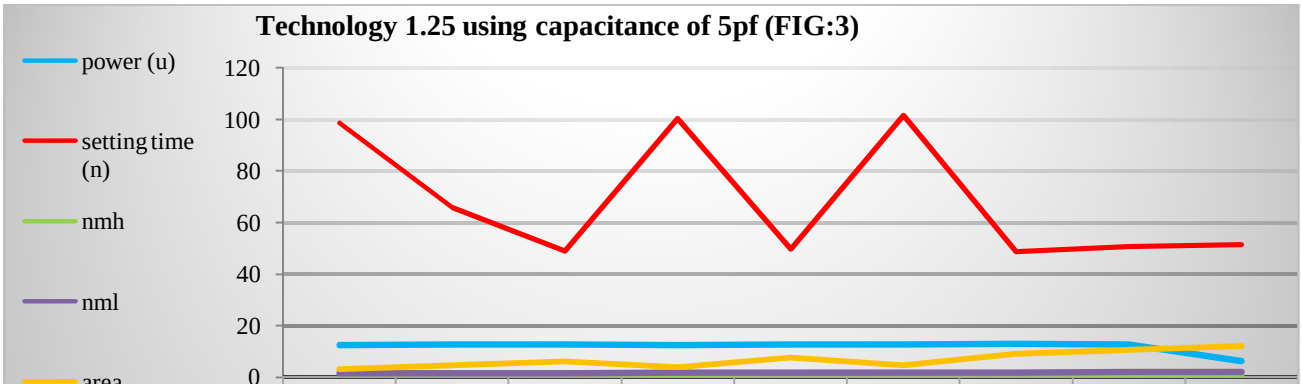
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	2.57	2.74	2.39	2.53	2.199	2.59	2.06	2.02	2.61
Settling time(n)	21.22	15.09	9.71	19.45	11.97	20.58	12.01	11.96	11.87
nmh	1.6	1.4	1.4	1.5	1.5	1.3	1.3	1.2	1.1
nml	1.6	1.6	1.6	1.7	1.6	1.9	1.8	1.9	2
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 1 On increasing the certain ratio, the power and setting time along with noise margin is high at expected ratios which future on decreases a ratio of 2 with future increase in ratio the power and settling time also increases at a ratio of 2.5 the power and settling is again to its minimum as shown in graph. .



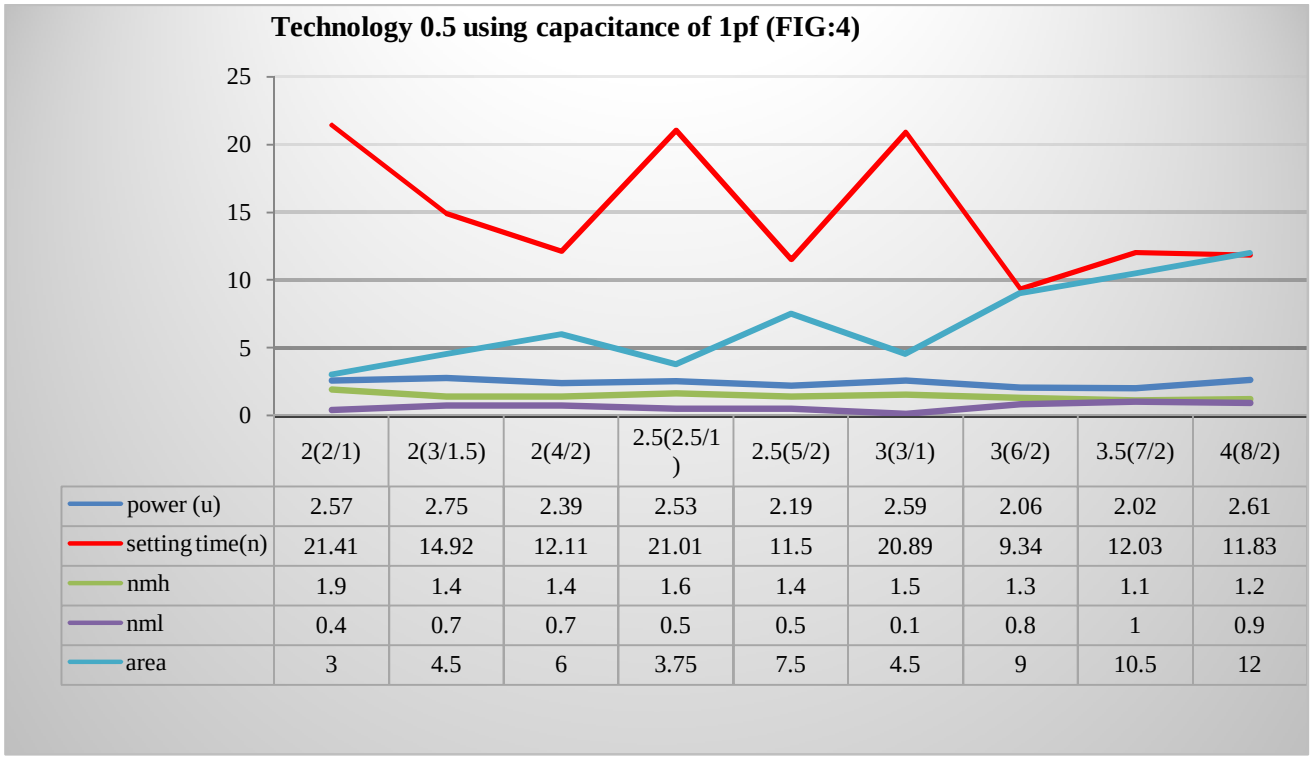
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	7.66	7.6	7.76	7.54	7.26	7.6	7.19	7.61	6.84
setting time (n)	52.61	41.5	29.24	58.89	29.24	60.54	28.53	28.21	29.89
nmh	1.4	1.5	1.4	1.4	1.4	1.2	1.4	1.2	1.1
nml	1.6	1.6	1.5	1.7	1.6	1.8	1.8	2	2
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 2 On increasing the certain ratio initially, the power and setting time along with noise margin is high at expected ratios which future on decreases a ratio of 2 with future increase in ratio the power and settling time also increases at a ratio of 2.5 the power and settling is again to its minimum as shown in graph.



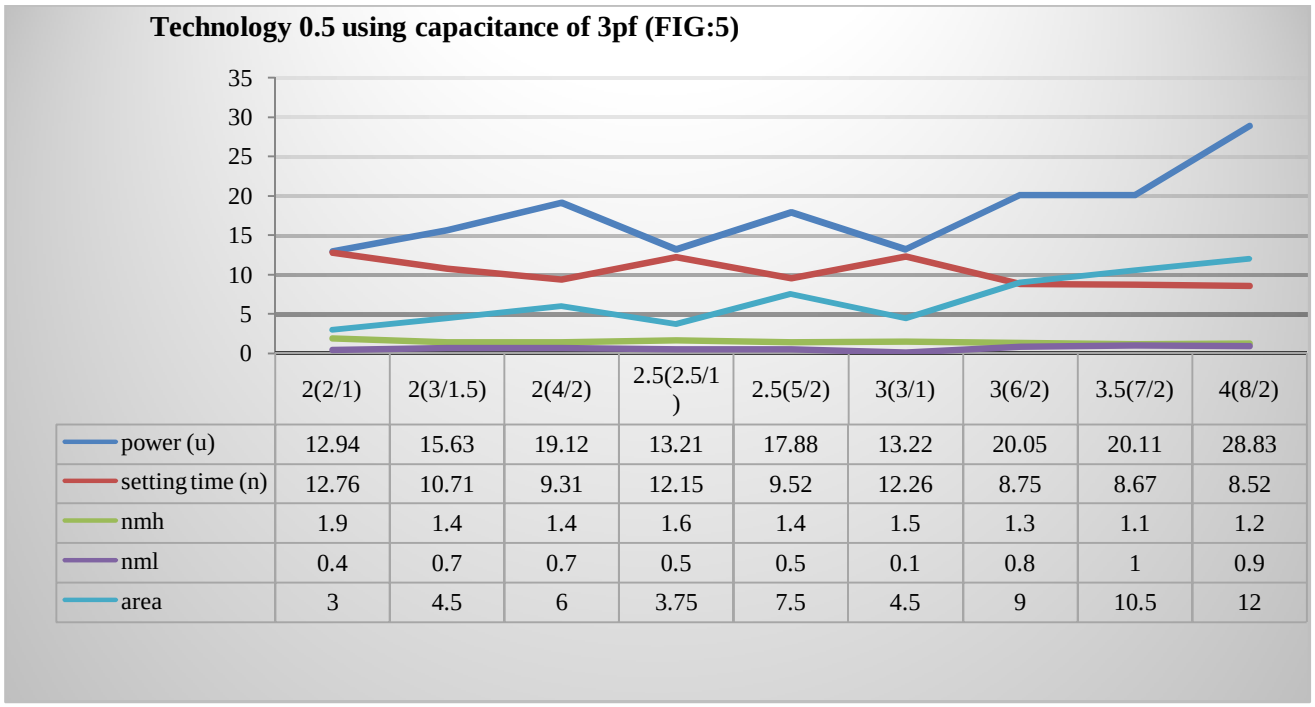
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	12.46	12.67	12.59	12.56	12.6	12.66	12.94	12.59	6.275
setting time (n)	98.6	65.79	48.9	100.33	49.52	101.51	48.63	50.55	51.38
nmh	1.5	1.5	1.4	1.3	1.4	1.4	1.5	1.2	1.2
nml	1.6	1.5	1.6	1.7	1.8	1.7	1.7	1.9	2
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 3 On increasing the certain ratio (PMOS (W/L)/NMOS (W/L) initially, the power and setting time along with noise margin is high at expected ratios which future on decreases a ratio of 2 with future increase in ratio the power and settling time also increases at a ratio of 2.5 the power and settling is again to its minimum as shown in graph.



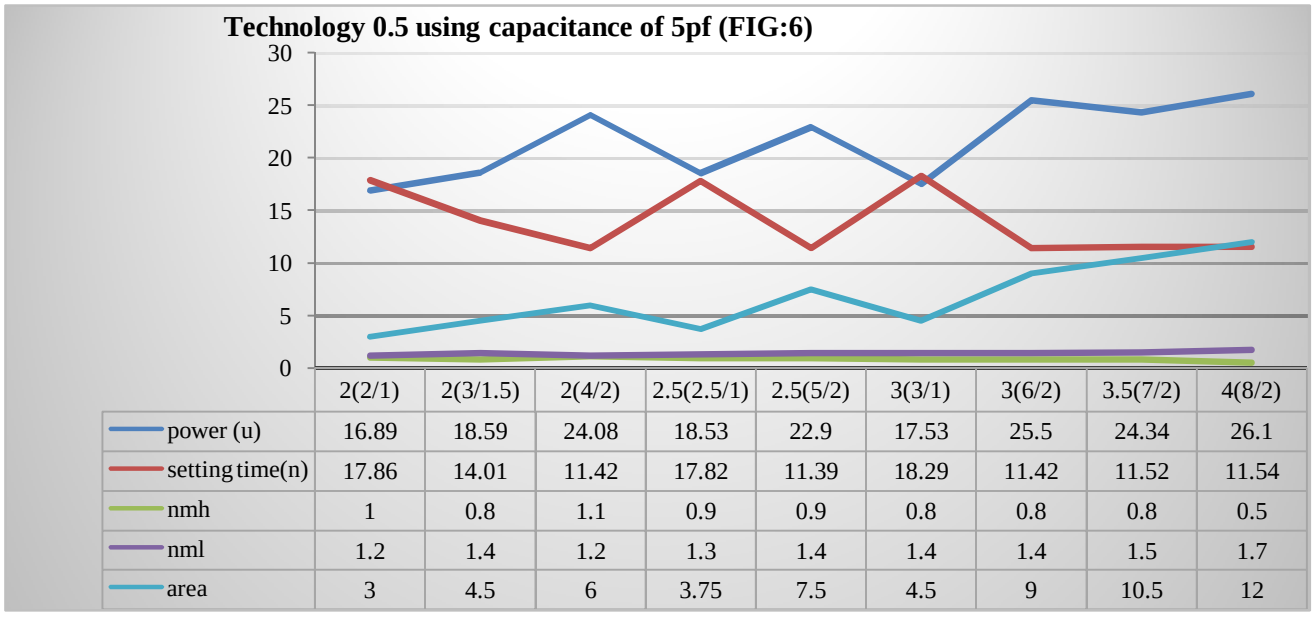
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	2.57	2.75	2.39	2.53	2.19	2.59	2.06	2.02	2.61
setting time(n)	21.41	14.92	12.11	21.01	11.5	20.89	9.34	12.03	11.83
nmh	1.9	1.4	1.4	1.6	1.4	1.5	1.3	1.1	1.2
nml	0.4	0.7	0.7	0.5	0.5	0.1	0.8	1	0.9
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 4 On increasing the certain ratio initially, the power and setting time along with noise margin is high at expected ratios which future on decreases a ratio of 2 with the future increase in ratio the power and settling time also increases at a ratio of 2.5. The power and settling time are less on future increasing certain ratio 3 power and settling time are high at the output and on the same ratio, with a different wavelength, we obtain minimum settling time along with noise margin and power is also low at the output as shown in above graph.



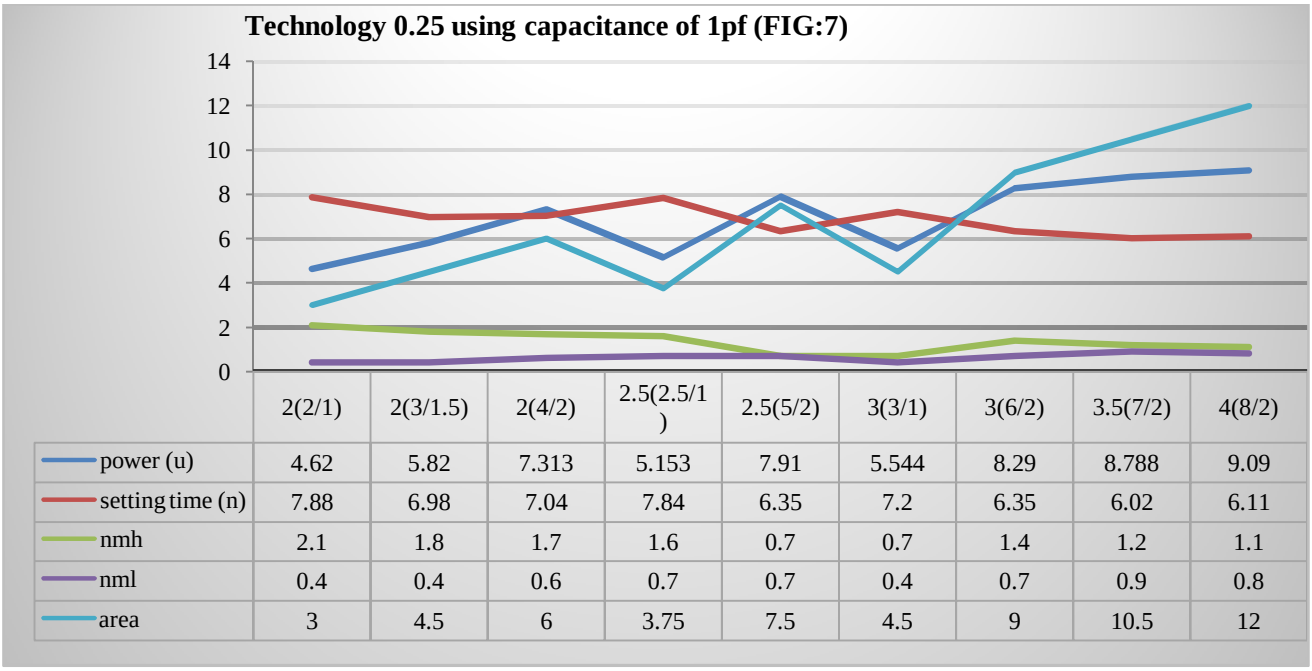
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	12.94	15.63	19.12	13.21	17.88	13.22	20.05	20.11	28.83
setting time (n)	12.76	10.71	9.31	12.15	9.52	12.26	8.75	8.67	8.52
nmh	1.9	1.4	1.4	1.6	1.4	1.5	1.3	1.1	1.2
nml	0.4	0.7	0.7	0.5	0.5	0.1	0.8	1	0.9
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 5 On increasing the certain ratio(PMOS/NMOS) initially, The power and setting time along with noise margin is high at expected ratios which future on decreases a ratio of 2 with future increase in ratio the power and settling time also increases at a ratio of 2.5 the power and settling time are less on future increasing certain ratio 3 power and settling time are high at output and on the same ratio with different wavelength we obtain minimum settling time along with noise margin and power is also low at output as shown in the above graph.



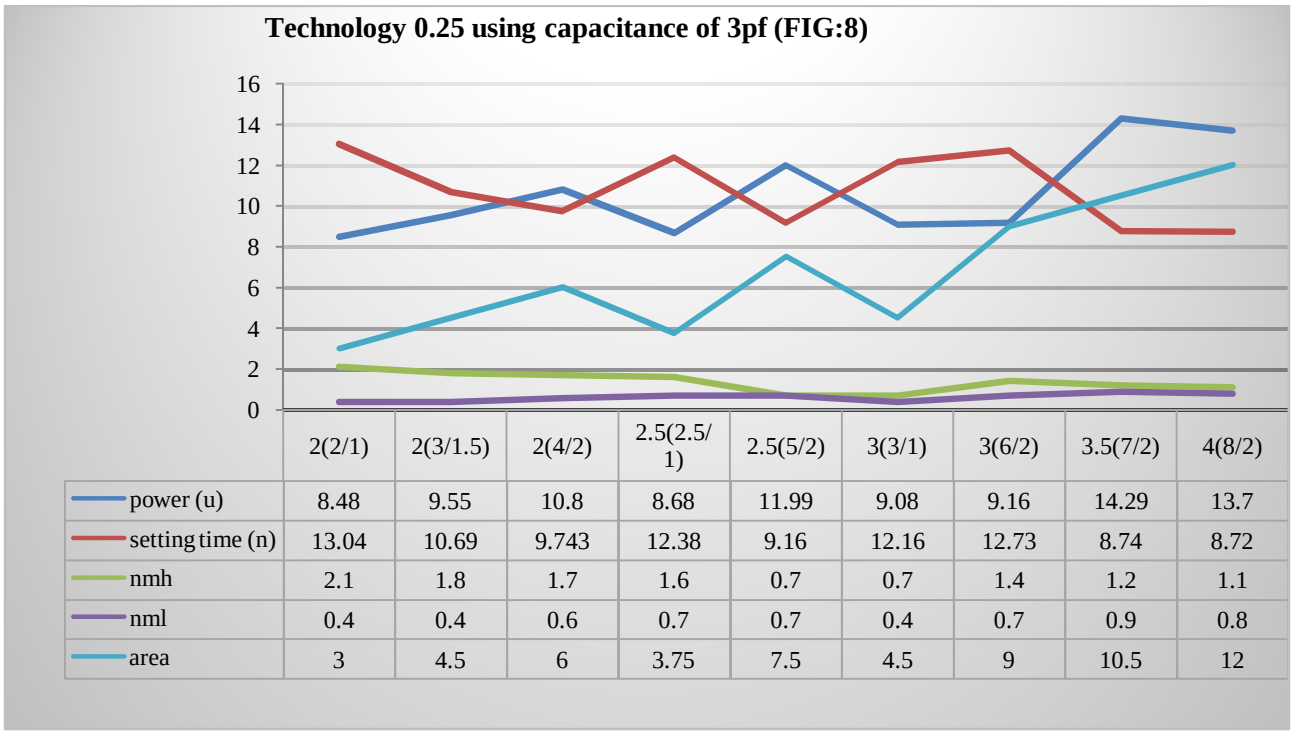
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	16.89	18.59	24.08	18.53	22.9	17.53	25.5	24.34	26.1
setting time(n)	17.86	14.01	11.42	17.82	11.39	18.29	11.42	11.52	11.54
nmh	1	0.8	1.1	0.9	0.9	0.8	0.8	0.8	0.5
nml	1.2	1.4	1.2	1.3	1.4	1.4	1.4	1.5	1.7
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 6 On increasing the certain ratio(PMOS/NMOS) initially, the power and setting time along with noise margin is high at expected ratios, which future on decreases at a ratio of 2 with a future increase in ratio, the power and settling time also increases at a ratio of 2.5. The power and settling time are less on future increasing certain ratio 3 power and settling time are high at the output and on the same ratio, with a different wavelength, we obtain minimum settling time along with noise margin and power is also low at the output as shown in above graph.



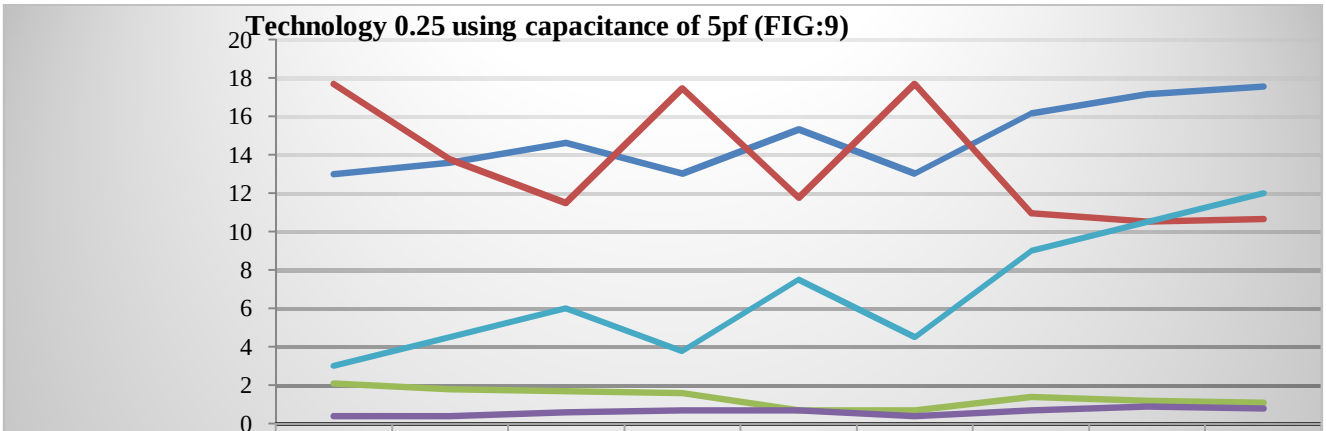
	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	4.62	5.82	7.313	5.153	7.91	5.544	8.29	8.788	9.09
setting time (n)	7.88	6.98	7.04	7.84	6.35	7.2	6.35	6.02	6.11
nmh	2.1	1.8	1.7	1.6	0.7	0.7	1.4	1.2	1.1
nml	0.4	0.4	0.6	0.7	0.7	0.4	0.7	0.9	0.8
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 7 On increasing the certain ratio (PMOS (W/L)/NMOS (W/L) initially, the power, area are low whereas the other parameter like settling time and noise margin is high, future increasing the ratio the all the parameters are seen too low a ratio of 2.5 future same conditions of minimum output of all parameters are obtained to be low at ratio 3 and future increase in ratio area and power at the output are observed to be high.



	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	8.48	9.55	10.8	8.68	11.99	9.08	9.16	14.29	13.7
setting time (n)	13.04	10.69	9.743	12.38	9.16	12.16	12.73	8.74	8.72
nmh	2.1	1.8	1.7	1.6	0.7	0.7	1.4	1.2	1.1
nml	0.4	0.4	0.6	0.7	0.7	0.4	0.7	0.9	0.8
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 8 On increasing the certain ratio (PMOS (W/L)/NMOS (W/L) initially, the power, area are low whereas the other parameter like settling time and noise margin is high, future increasing the ratio the all the parameters are seen to low at a ratio of 2.5 future same conditions of minimum output of all parameters are obtained to be low at ratio 3 and future increase in ratio area and power at the output are observed to be high.



	2(2/1)	2(3/1.5)	2(4/2)	2.5(2.5/1)	2.5(5/2)	3(3/1)	3(6/2)	3.5(7/2)	4(8/2)
power (u)	13	13.61	14.62	13.02	15.34	13.03	16.16	17.16	17.55
setting time (n)	17.69	13.74	11.5	17.47	11.74	17.69	10.94	10.52	10.65
nmh	2.1	1.8	1.7	1.6	0.7	0.7	1.4	1.2	1.1
nml	0.4	0.4	0.6	0.7	0.7	0.4	0.7	0.9	0.8
area	3	4.5	6	3.75	7.5	4.5	9	10.5	12

Figure 9 On increasing the certain ratio initially, the power, area are low whereas the other parameter like settling time and noise margin is high, future increasing the ratio the all the parameters are seen to low at a ratio of 2.5 future same condition of minimum output of all parameters are obtained to be low at ratio 3 and future increase in ratio area and power at the output are observed to be high.

8. RESULTS AND CONCLUSION

As shown in all figures for different values of the expected ratio of transistors, we get different values of all the parameters. It has been observed that technologies and fixed values of capacitive load (on-chip inverter has a fixed value of load capacitance) plays an important role in CMOS inverter designing. In case of different technologies, optimum results are obtained at different expect ratio of transistors. Similarly different expect ratios are required to be set to get optimum values of different parameters for different load capacitors.

Designing techniques for CMOS inverter reported in the literature have not considered, load capacitance and technologies while searching for all the parameters. In this work, we have shown that by considering the technology and fixed load capacitor optimum power dissipation can be obtained with reasonable values of settling time, noise margin, area and power.

REFERENCE

[1] “International Technology Roadmap for Semiconductors,” Semiconductor Industry Association, 2005.
[2] “Wayne Wolf,” Modern VLSI Design, 3rd Edition 4th Edition prentice hall publication 2008.